PATENT
Docket No. Intel/17225

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Tian et al.	)	I hereby certify that this paper is
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Serial No.: 10/677,414	)	States Postal Service with
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	)	Commissioner for Patents, P.O.
Assignee: Intel Corporation	)	Box 1450, Alexandria, VA 22313-
	)	1450 on this date:
For: "Methods And Apparatus For Reducing Memory Latency In A Software Application"	)	**February 13, 2006**
	)	Michael W. Zimmerman
Group Art Unit: 2121	)	Registration No.: 57,993
	)	Agent for Applicant(s)
Examiner: Unknown	)	

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The patents and/or publications listed on the enclosed PTO Form-1449 are submitted pursuant to 37 CFR §§ 1.56, 1.97, and 1.98. Copies of the patents or publications are enclosed.

Submitted herewith is a copy of an Official Search Report of the PCT Patent Office in parent/counterpart foreign application No. PCT/US2004/032212 filed September 29, 2004.

TIME OF FILING

This information disclosure statement is being filed, to the best of the undersigned's knowledge, before the mailing date of a first Office action on the merits. In accordance with 37 CFR §1.97(b), no certification or fee is required.

METHOD OF PAYMENT

No fee is required.

The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 50-2455. A copy of this paper is enclosed.

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Respectfully submitted,

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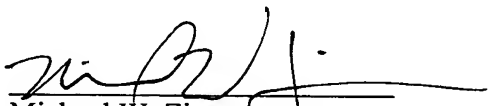
By: 

Michael W. Zimmerman
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February 13, 2006

Agent for Intel Corporation

Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. Intel/17225	Serial No. 10/677,414
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		Applicant Tian et al.	
		Filing Date **October 2, 2003**	Group Art Unit 2121

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)		
	C01	International Search Report for International application no. PCT/US2004/032212 published with publication no. WO 2005/033926 A3, April 14, 2005
	C02	Dorai et al., *Optimizing SMT Processors for High Single-Thread Performance,* Journal of Instruction Level Paralelism 5 (2003), April 2003, pp 1-35.

EXAMINER	DATE CONSIDERED
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	